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2020 DOE Vehicle Technology Office Annual Merit Review

Next-Generation, High-Temperature, High-Frequency, High-Efficiency, High-Power Density Traction System

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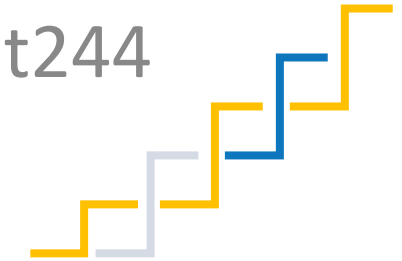
Project ID: elt244



This presentation does not contain any proprietary, confidential, or otherwise restricted information.

Overview

- Timeline: 6/1/2019 – 6/1/2024
- Budget/Spend Plan
  - Total Cost: $1.5M
  - FY 2019: $300k
- Milestones
  - Preliminary design validated
  - Thermal and PCB co-design completed
  - Low-level control tested
  - Inverter cost ≤ $2.7/kW
  - Inverter power density ≥ 100 kW/L
  - Demo hardware at 100 kW peak
- Barriers (EETT 2025 Roadmap)
  1. *WBG device power and voltage levels and availability*
  2. *WBG multi-physics integration designs to enable optimal use*
  3. *Component optimization for miniaturization and cost reduction.*
  4. *Low inductance requirements for WBG multi-physics integration*
- Partners
  - National laboratories and university partners

Relevance

- The U.S. DRIVE Partnership Goal to advance electric vehicles requires a compact, high-performance and cost-effective electric traction drive system
- The proposed inverter architecture has several unique features that can be exploited in advanced EV drivetrains
  - Can drive low-inductance and high electrical frequency machines
  - Can compensate for machine non-idealities (e.g., torque ripple in switched reluctance machines)
  - Reduces EMI filters and DC-link capacitors
  - Fast transient response capability (e.g. during braking and acceleration)

Objectives (EETT 2025 Roadmap)

- **Cost**: < $2.7/ kW through novel circuit topologies, component identification and characterization, and packaging
- **Technical target**: > 100 kW/L traction inverter, compatible with next-generation low-weight (and low-inductance) electric machines
- **Target demonstration** [1] :
  - Build 100 kW inverter demonstrator
  - Integration into vehicle cooling loop (85°C)
  - Integration with advanced electric machine
  - Experimental and analytical validation of system-level redundancy and reliability

[1] Overall objective: hardware demonstrator meets APIM (min) or Scalability (reach) target from Appendix A of EETT Roadmap.

Milestones Overview

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Year 1		
Milestone	**Type**	**Description**
High level specifications completed	**Technical**	**High level traction inverter specifications completed** ✓ EETT APIM targets; topology is compatible with arbitrary motor
Evaluation of components completed	**Technical**	**Evaluation of semiconductor devices and passive components (e.g. inductors and capacitors) completed** ✓ MLCC and GaN
Multi-objective optimization completed	**Technical**	**Multi-objective design optimization to determine circuit topology and switching frequency completed** ✓ Updated for next-gen
Simulation completed	**Technical**	**Simulation demonstrating phased-shifted PWM operation, and balanced capacitor voltages** ✓ PLECS & MATLAB models OK
Preliminary design validated	**Go/No Go**	**Assessment of preliminary design completed, verifying electric drive inverter with power density > 100kW/L is achievable**
Year 2		
Milestone	**Type**	**Description**
PCB design completed	**Technical**	**Full PCB design completed, meeting system size targets** ✓* Lessons learned from Y1 directly applicable
PCB fabrication completed	**Technical**	**PCB passes all design for manufacturing requirements, sent to board house** ✓* CM assembly of qty (12) Y1 15 kW-scale modules
Subsystem assembly completed	**Technical**	**Assembly of hardware prototype completed** ✓* Lessons learned from initial Y1 array will contribute to this revision and process
Low-level control development completed	**Technical**	**Control code to demonstrate phase-shifted PWM operation of transistors** ✓* Control prototyped on a 9-module 3-phase system
Initial hardware prototype completed	**Go/No Go**	Initial hardware prototype fully functional, with sinusoidal output voltage, balanced capacitor voltages and state feedback
Year 3		
Milestone	**Type**	**Description**
Thermal modeling completed	Technical	Detailed thermal model of PCB developed, including thermal vias and thermal interface material to cold-plate
Cold-plate design completed	Technical	Initial cold-plate design completed, meeting converter cooling targets
Converter thermal modeling surrogate completed	Technical	Thermal replica of power converter completed, using diode-connected GaN devices to act as controllable heat sources
Cold-plate manufacturing completed	Technical	Hardware prototype of cold-plate design completed, with custom milled spacing for semiconductors
Thermal and PCB co-design completed	**Go/No Go**	Hardware demonstration with thermal management solution (cold-plate cooling GaN devices, corresponding to >98% efficiency
Year 4		
Milestone	**Type**	**Description**
Baseline on-board converter metrics established	Technical	Determine baseline power density and efficiency target using update state-of-the-art commercial prototypes as benchmarks
Modeling and simulation supporting target numbers	Technical	Detailed simulation and loss modeling supporting power density and efficiency target
PCB layout completed	Technical	Full converter PCB design completed, passing all manufacturing design constraints
Thermal design completed	Technical	Thermal management solution (air or liquid cooled design, TBD) completed, supported by finite element analysis
On-board power converter design competed	**Go/No Go**	Full CAD files and supporting model verification of on-board power converter. Meets all design targets
Year 5		
Milestone	**Type**	**Description**
On-board converter assembly completed	Technical	Hardware prototype fully assembled, electrical and thermal
Control code completed	Technical	Digital control completed, confirmed working on hardware converter
Testing and validation completed	Technical	All electrical and thermal characterization completed, captured in design report
Efficiency and power density targets achieved	Technical	Aggressive power density and efficiency numbers (determined in consultation with DOE staff and consortium partners) achieved.

✓ 17.4 kW/L @ 13.4 kW

Approach – Novel Topology

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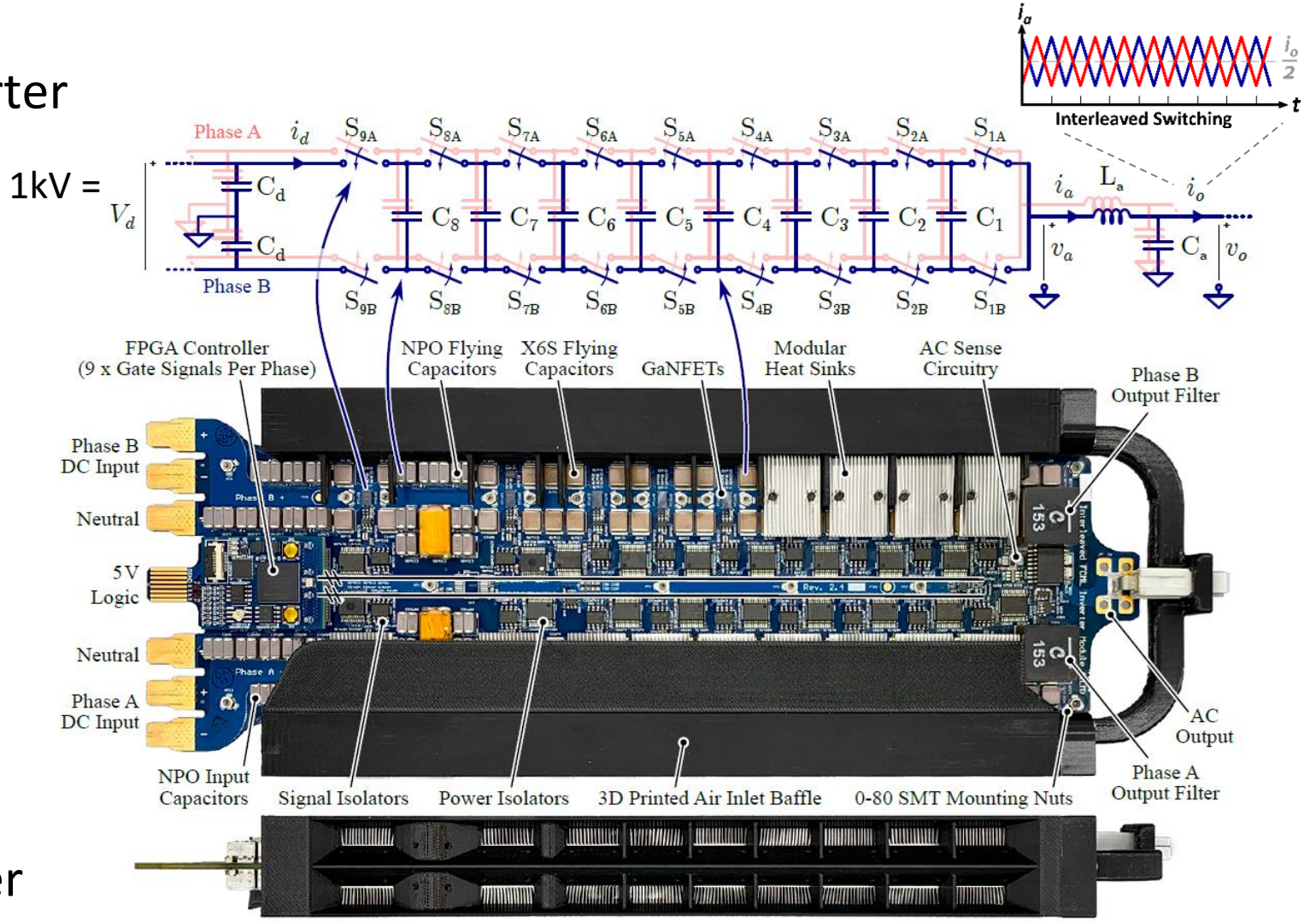
Flying Capacitor Multilevel Converter

- Energy dense capacitors are used in power processing
- Multilevel operation, high effective frequency reduces required filter for a given THD
- Wide-bandgap devices facilitate fast switching, low losses and compact design
- High switching frequency reduces the size of the power processing capacitors
- Dual-interleaved design further reduces filter requirements



Y1 15 kW-scale Hardware Prototype

New Capabilities with This Approach

- Proposed inverter architecture has several unique features that can be exploited in new electric machine designs
  - Very low THD sinusoidal output voltage capabilities
    - Can drive extremely low inductance machines
  - Arbitrary output waveform capabilities
    - Can compensate for machine non-idealities (e.g., torque ripple in switched reluctance machines)
  - Very high switching frequency (> 100 kHz)
    - Dramatic reductions in EMI filters and DC link capacitor requirements
    - Very fast transient response during braking and acceleration
  - Possibility to operate at very high modulation frequency (> 10 kHz)

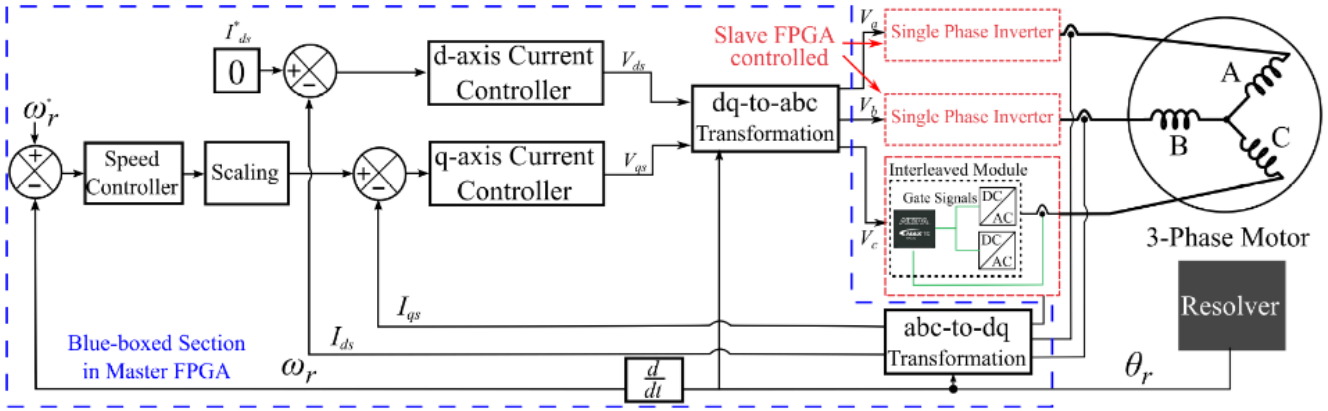
Approach – Scalability & Redundancy

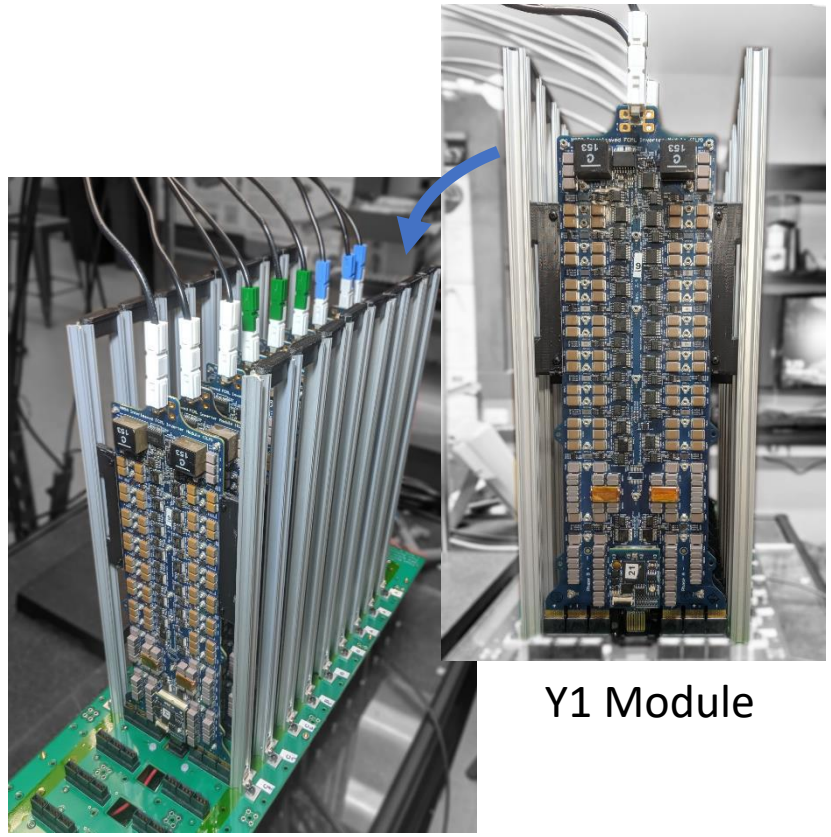
Individual modules rated to a fraction of the total power

- Simplifies design, manufacturing and test scope, with individual modules optimized based on loss-model and volume cost functions (*barrier 2*)
- Modules can be paralleled for more phases or current
- Potential reliability boost through redundant hardware

Hierarchical control coordinates drive behavior

- Local controllers run PWM, balance interleaved currents
- Master controller delegates torque commands
- Shedding modules may improve light-load efficiency



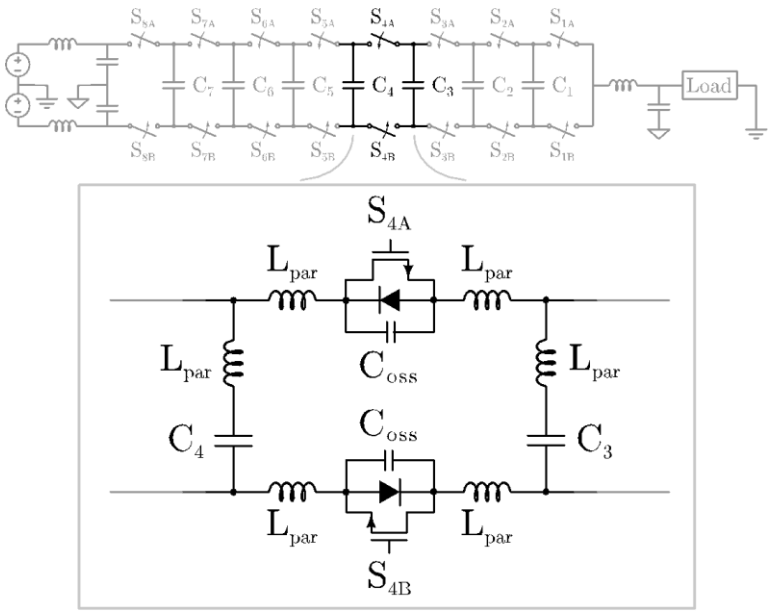


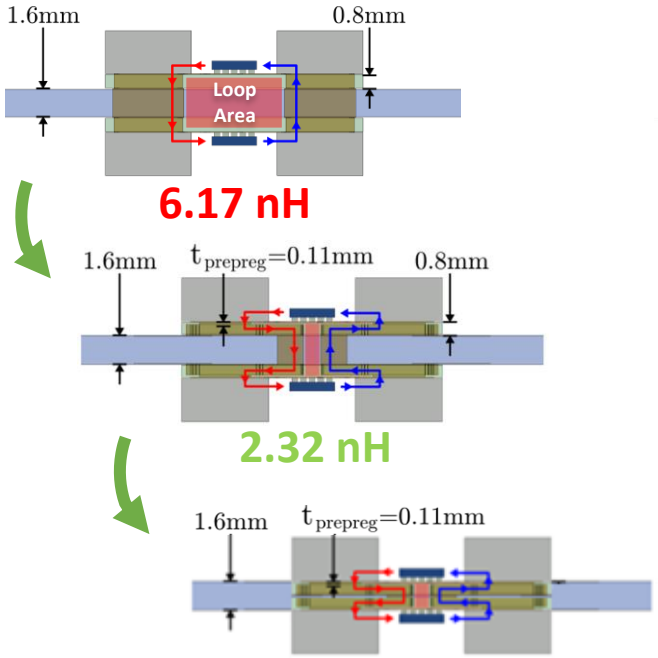
Y1 Module

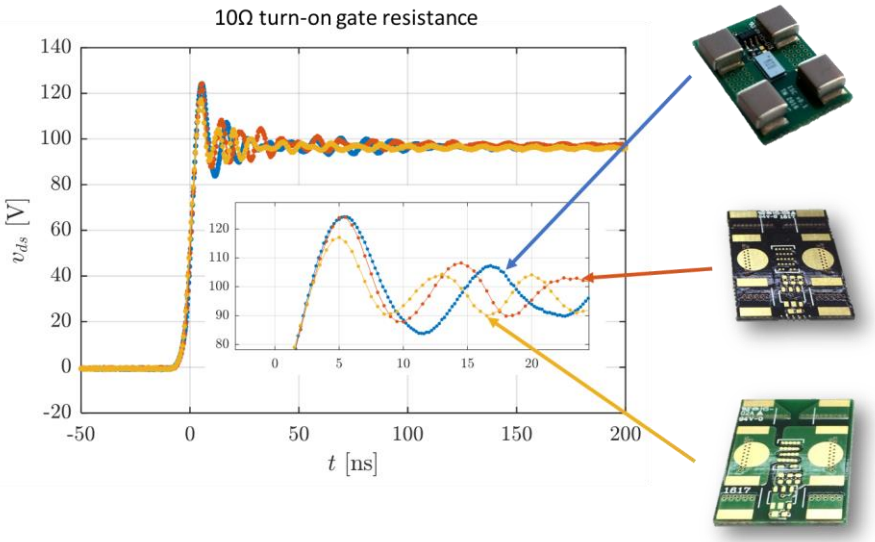
Y1 Array

Approach – Packaging

- FCML yields high-voltage clearance with low-voltage, wide-bandgap devices (*barrier 1*)
- Compact layouts are possible with standard, cost-effective PCB manufacturing (*barrier 3*)
- Multiphysics simulation (3D FEA, Monte-Carlo modeling) and experimental validation of electrically-thin technique reduces parasitic inductances (*barrier 4*)
- Decreased overshoot and ringing amplitude can also reduce EMI



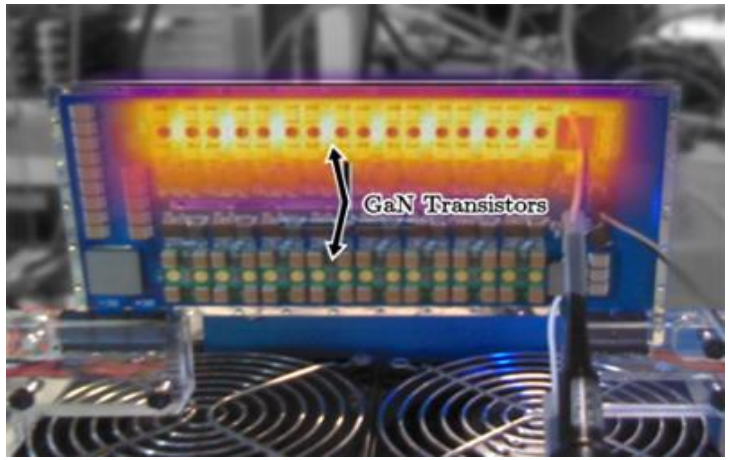




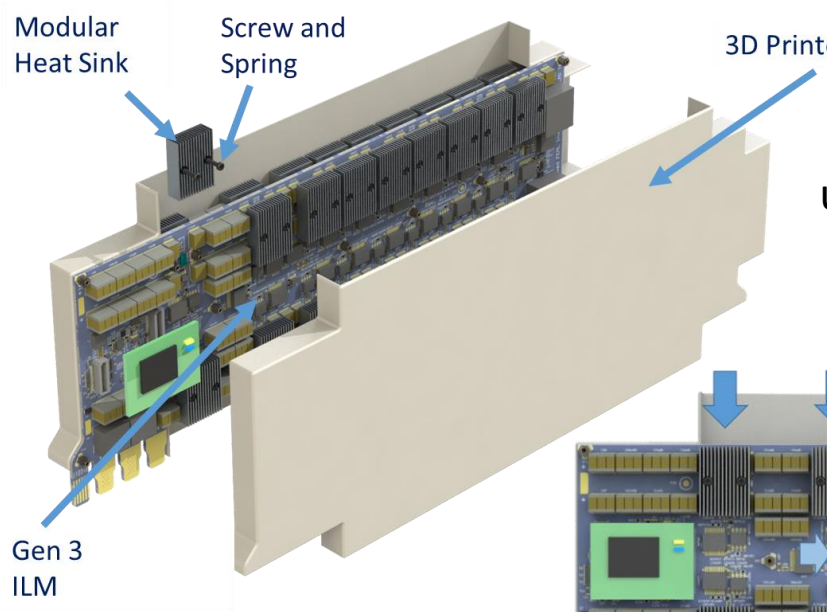
FY19 Hardware **<1 nH (est)**

Approach – Thermal Design

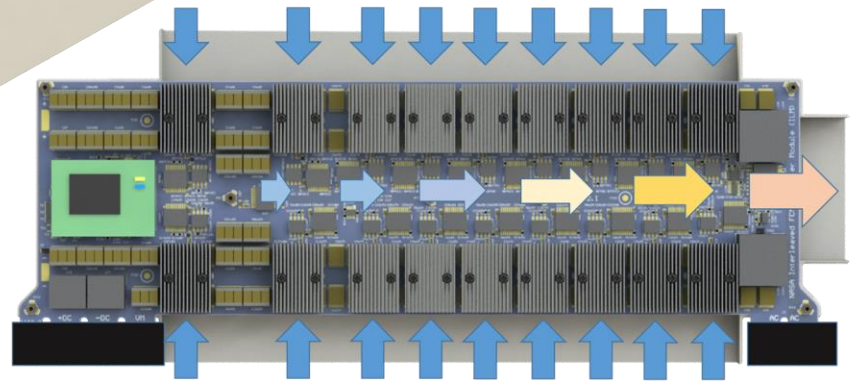
- Increased number of active devices provides intrinsic heat-spreading effect
- CFD-optimized modular heat sinks allows for use of higher performance TIM without compromising GaN chips with mechanical stress from uneven pressure across PCB
- Next steps will extend the approach to liquid cooling for greater performance



Composite thermograph highlighting the heat spreading properties of the converter



A modular, air-cooled approach used to demonstrate the topology, but can quickly adapt to liquid cooling for greater performance.

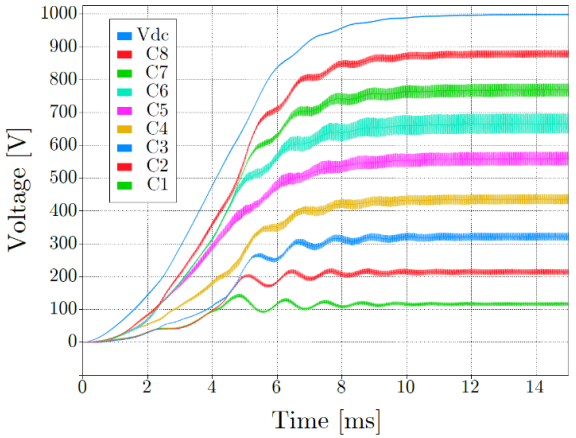


Accomplishments – Start-Up

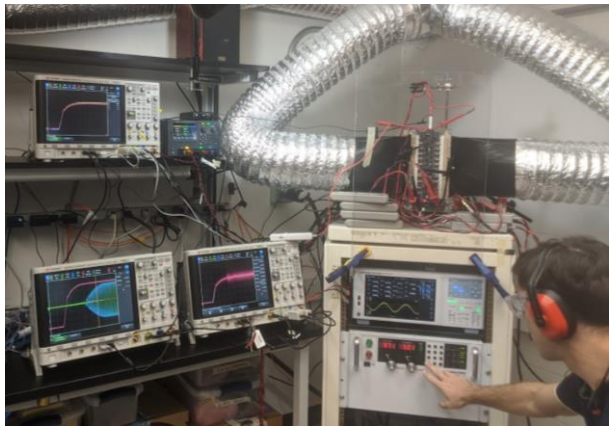
- Balanced DC bus start-up has been a key challenge associated with the topology [1]

- Changing the modulation mode and leveraging existing converter components provides a simple and robust startup
- A precise PLECS model that captured the non-linear dynamics of the capacitor network demonstrated feasibility
- The hardware prototype successfully verified the start-up method, achieving 1kV DC bus, balanced capacitor voltages and 5 kW AC output power in < 1 s
- Published in 2020 IEEE Applied Power Electronics Conference and Exposition

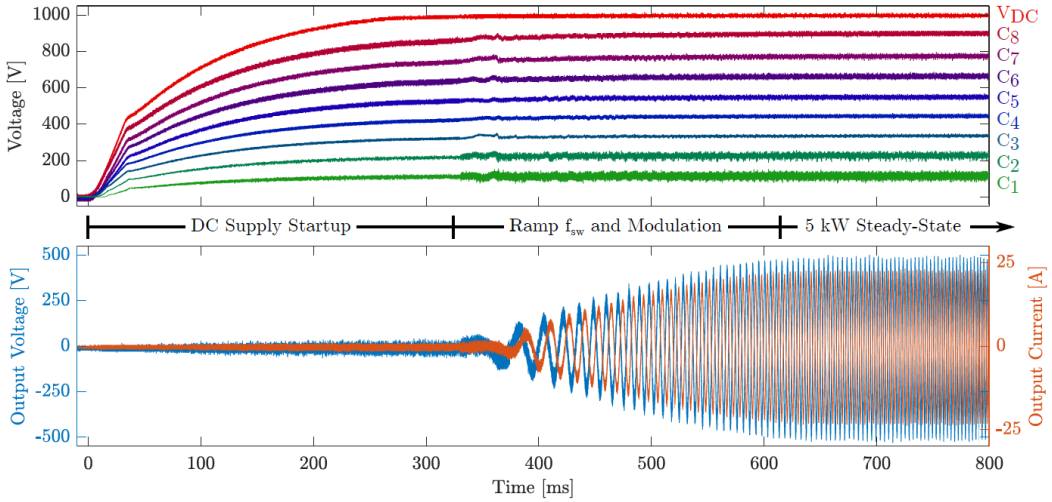
PLECS Simulation



Experimental Setup



Experimental Results

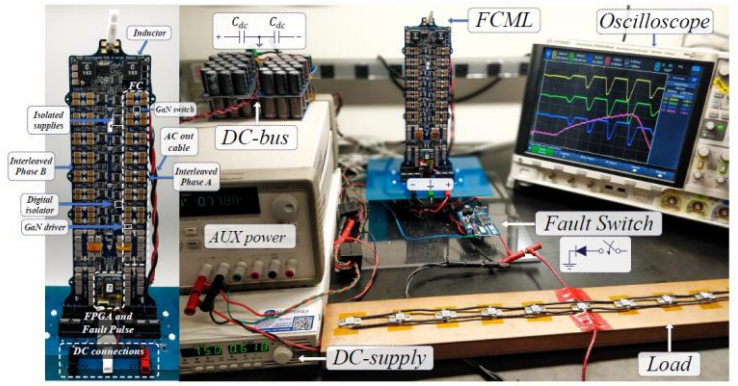


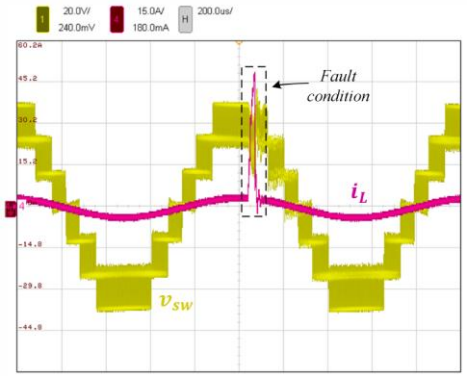
[1] The question of what challenges may arise during start-up was raised at the June 2019 Consortium Meeting at ORNL.

Acc. – Fault Analysis and Mitigation

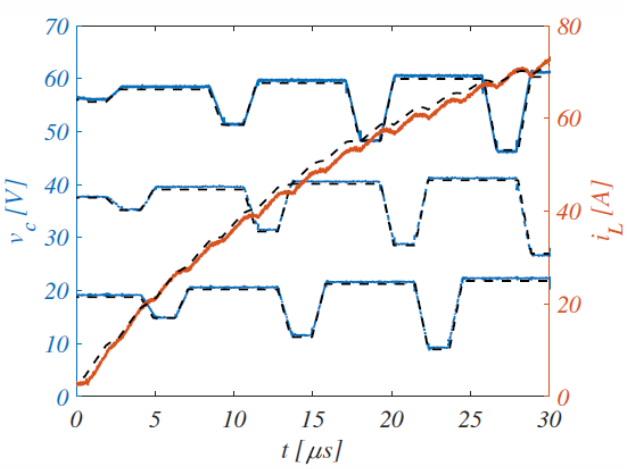
- Converter short-circuit detection and ride-through capability serves the reliability goals set forth in the EETT 2025 Roadmap
- A new analytical model was developed to study short-circuit behavior, which had not been explored in prior work
- PLECS circuit simulations demonstrated the accuracy of the analytical model
- Short-circuit tests were conducted on the project hardware prototypes, and experimentally validated the model
- Analog and digital logic was developed to quickly detect a short-circuit at the output
- A mitigation strategy based directly on the technique used in start-up was proposed, simulated and experimentally validated

Short-Circuit Experimental Setup

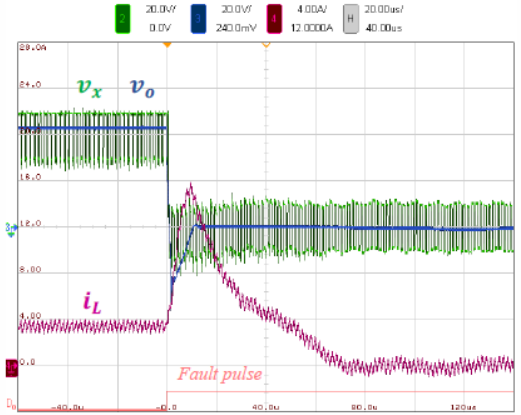




Short-Circuit Model (dashed) and Experiment (solid)



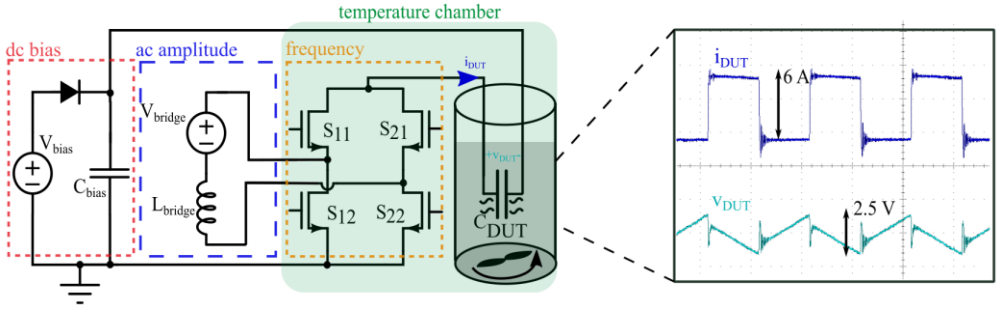
Experiment Illustrating Detection and Mitigation



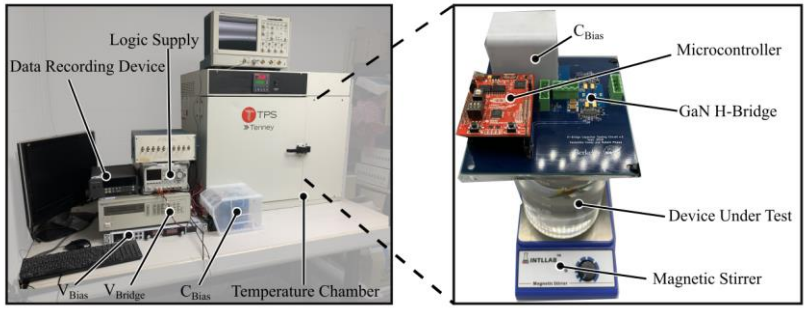
Acc. – Component Characterization

- Typical capacitor characterization is performed under small signal operation; less valuable for high-power applications
- A custom circuit was designed such that frequency, DC bias and large-signal AC amplitude can be swept for analysis
- Calorimetry results were collected and compared against several loss models derived from material properties
- This data can be used to better understand performance under realistic operating conditions and directly feed the next-generation converter design
- Published in 2020 IEEE Applied Power Electronics Conference and Exposition

Electrical Excitation Circuit

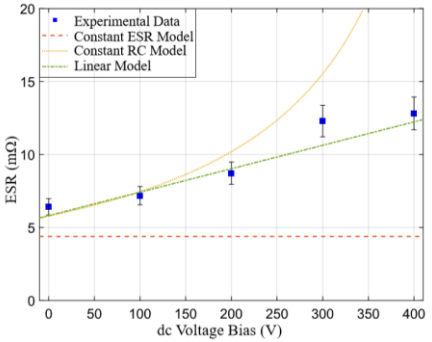


Calorimetric Setup



Model Comparison and Calorimetric Data

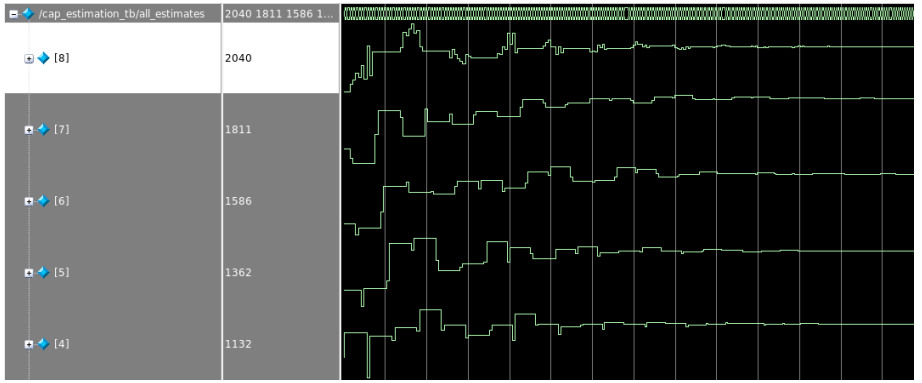
Model	Accuracy	Complexity	Effort
Constant ESR	✗	✓	✓
Constant RC	✗	✗	✓
Linear Model	✓	✓	✗



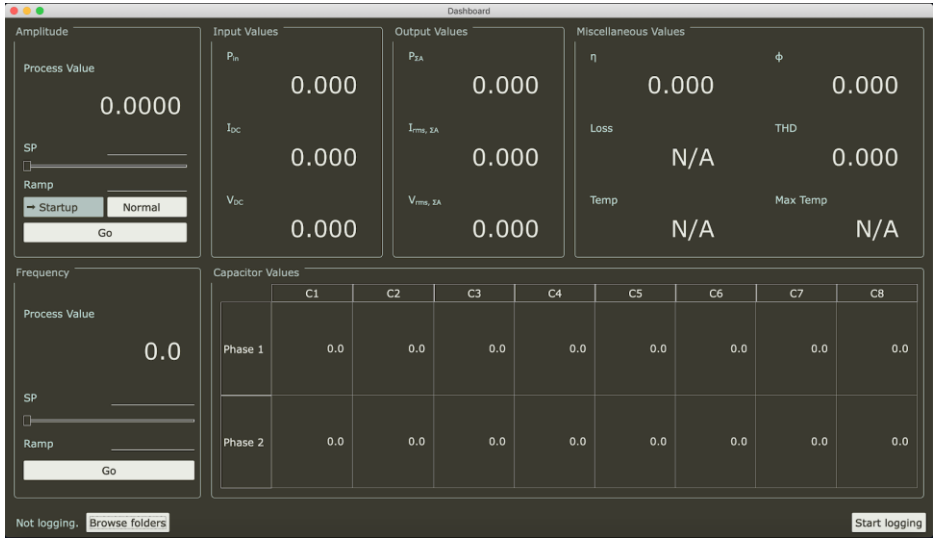
Acc. – Firmware/Software

- An FPGA provides low-level control
- This processing capability is leveraged to provide state estimation and fault detection from fewer sensors
- High data-rate communication blocks allow estimations and measurements from the controller to be sent at a over an electrically isolated link to a computer
- A custom Python interface leveraging open-source libraries allows for on-line control and polling of both converter measurements and bench equipment.
- Feature development and debug can be safely performed without connecting a debugger directly to the converter
- Can be quickly expanded for full array

Capacitor Estimation Block Validation in ModelSim

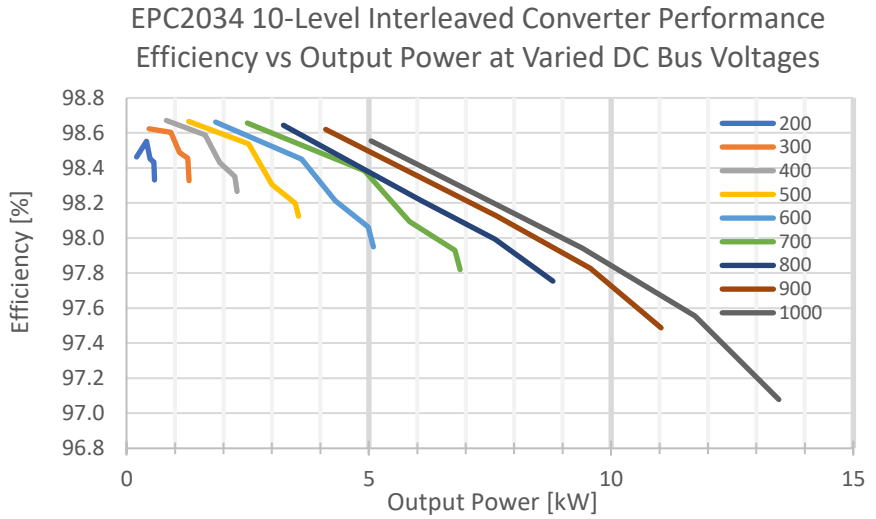


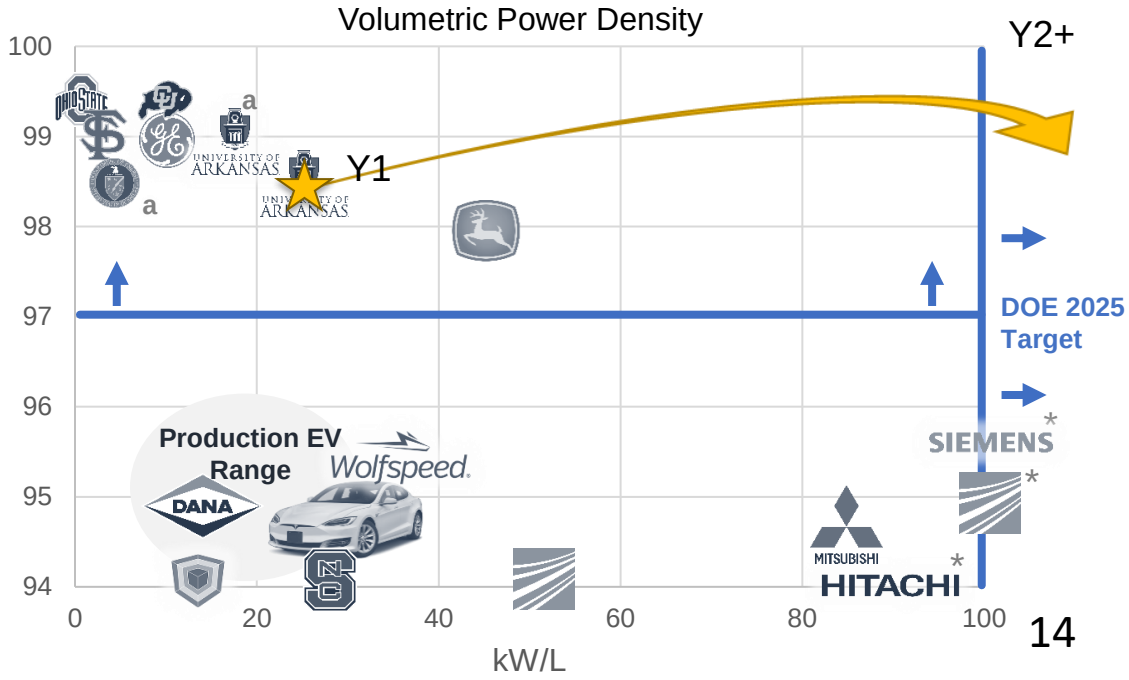
GUI with Modulation Commands and Readings



Acc. – High Power Results

- A single, air-cooled inverter module with a 1 kV DC bus was tested to 13.4 kW into a variable resistive load bank
- Represents highest efficiency and power density sine-output, air-cooled inverter
- Thermocouple measurements confirm GaN operation at > 100°C, but indicate imperfect heat sinking to devices
- Improvements to heat sink assembly and closed-loop control are expected to boost efficiency and power output further





Response to Reviewers' Comments

This is the first year of this project.
There are no prior reviews.

Collaboration and Coordination

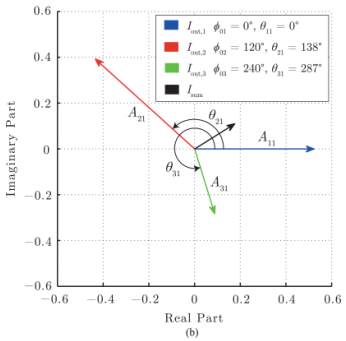
- Consortium members (e.g., Purdue, Wisconsin for machine integration)
  - Looking for ideas of how to engage virtually given travel limitations
- National laboratories
  - Sandia for WBG expertise and packaging
  - ORNL for vehicle integration
- OEM partners
  - Looking for guidance on this aspect
  - Well connected with existing industry partners; could be more heavily involved
- Component suppliers
  - GaN Systems, EPC, Infineon, Texas Instruments, TDK, Murata

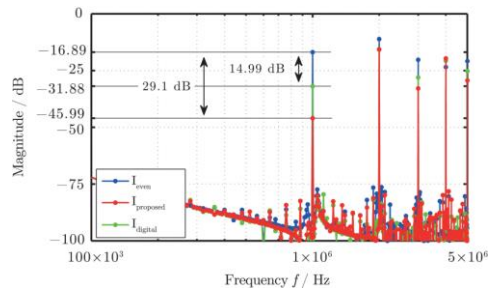
Remaining Challenges and Barriers

- Automotive qualified GaN transistors
  - There could be possible delays in approval, and limited supply
- Component-level reliability data may be incomplete
  - State-of-art devices may lack abundant reliability data
- Effects of temperature and vibration on the current design are unknown
  - Though power-dense, MLCCs and chip-scale devices should be tested further
- Remaining years:
  - High power testing requires infrastructure setup (currently up to 20 kW in-house)
  - Electrical communication between a large number of transistors and inverter modules can be challenging; additional research needed to ensure signal integrity
  - Integration with liquid cooling requires domain expertise and additional hardware capabilities, but is very promising given our results with air-cooling only
  - System level testing requires integration between geographically separated teams

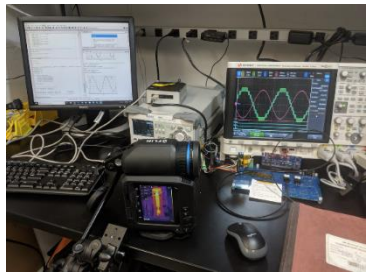
Proposed Future Research

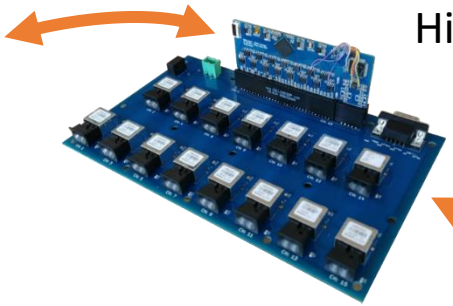
- **Electromagnetic interference testing**
  - Advanced PWM on the inverter array may further reduce filtering requirements
  - Facilitates scalability and integration
- **Hierarchical control development**
  - FPGA code, optical link have been tested
  - Develop a C co-processor for motor control, and electrical link for communication
  - Facilitates scalability, collaboration and the use of the hardware as a platform
- **Liquid heat-exchanger or immersion-based thermal management**
  - Leverage the benefits of the air-cooled modular approach for liquid cooling
  - Facilitates Y3 milestones



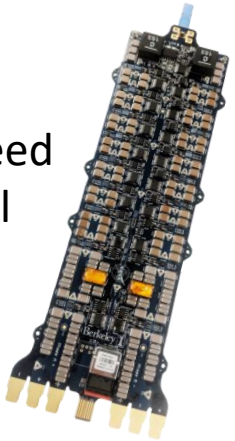


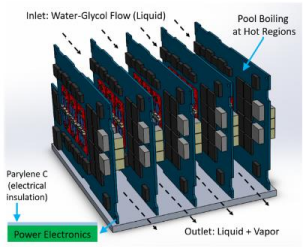
High-Speed USB <-> SPI (FTDI)

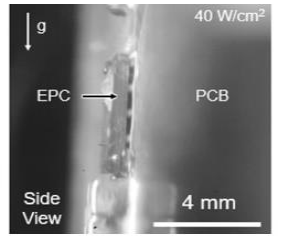


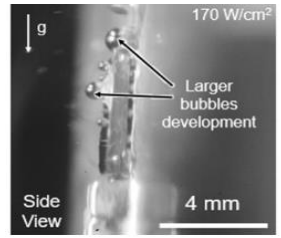


High-Speed Optical UART





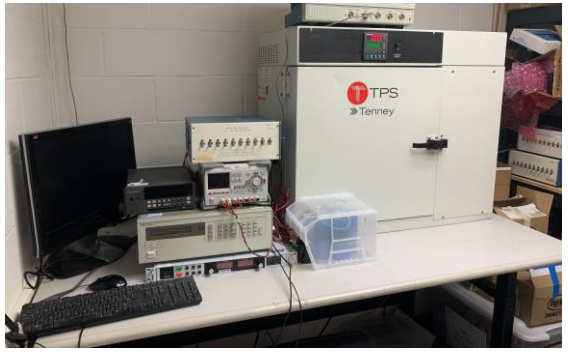


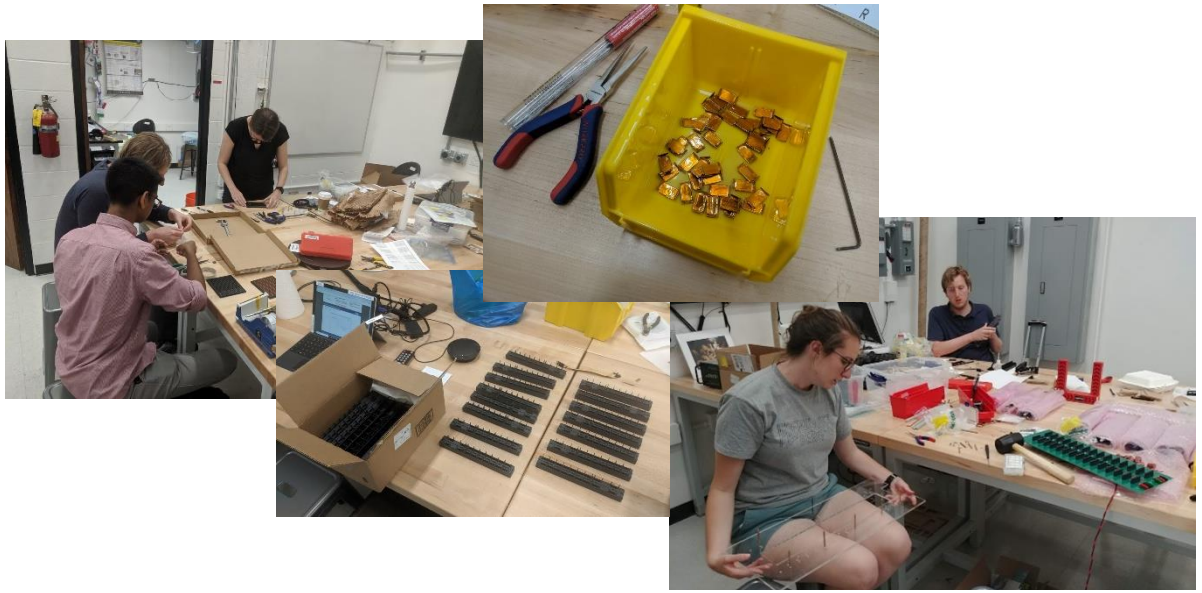


Any proposed future work is subject to change based on funding levels.

Proposed Future Research

- **Accelerated lifetime testing of modules**
  - Temperature cycling and vibration tests against relevant standards (e.g. SAE J1455)
  - Retire risks associated with new or unconventional component selection
  - Informs additional manufacturing requirements (e.g. device underfill) for Y2+
- **Improve module ease of assembly**
  - Standard PCB assembly currently employed is simpler than traditional power module assembly, but challenges remain
  - Iterate on packaging for faster and more reliable mechanical and thermal contacts
  - Informs Y2+ designs and path to market

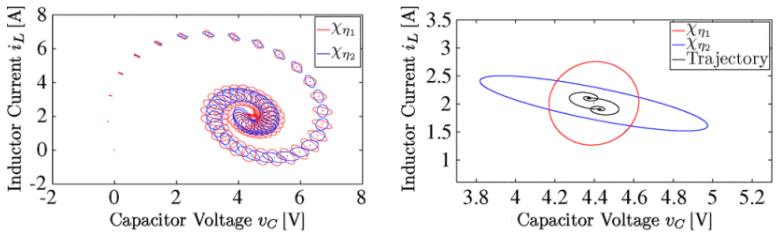




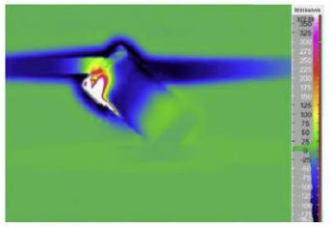
Any proposed future work is subject to change based on funding levels.

Proposed Future Research

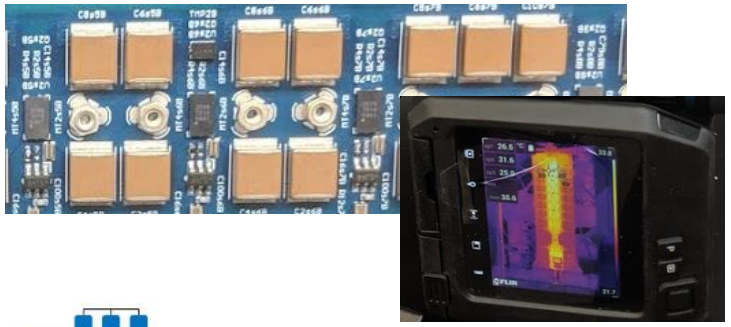
- **On-line fault detection and mitigation**
  - Extend Y1 output short-circuit fault study
  - Define limits of on-line failure coverage
  - Facilitates reliability goals
- **Converter-level, lock-in IR inspection of GaN devices and MLCC capacitors**
  - Non-invasive detection of assembly and lifetime issues on assembled PCB
  - Facilitates reliability goals
- **Synthesis top-down and bottom-up failure models during design stage**
  - System reliability as a function of converter optimization (e.g. level count)
  - Facilitates reliability goals

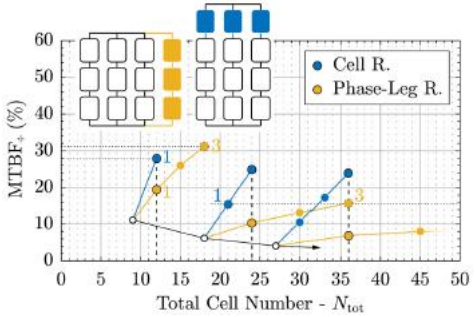


Hope et al. IEEE Tr. Cir. & Sys. 2011



Andersson et al.
JESTPE 2018





M. Guacci, et al.
IEEE ECCE 2018

Any proposed future work is subject to change based on funding levels.

Summary

- Enable dramatic cost and size reduction in EV traction inverters through new circuit topologies, which can exploit low-voltage (e.g., GaN) transistors in a high-voltage applications
  - Reduced passive component size
  - Conventional PCB-style hardware
  - Improved cooling through distributed heat generation
- Further the understanding and control of FCML converter dynamics under various motor operating points and transients
- Seek to rapidly demonstrate concepts and performance in hardware
- Execute key DOE research objective of training students

6 grad: Nathan Pallo, Samantha Coday, Logan Horowitz, Joseph Schaadt, Mads Taul, Chris Barth

2 undergrad: Avinash Jois, Amanda Jackson

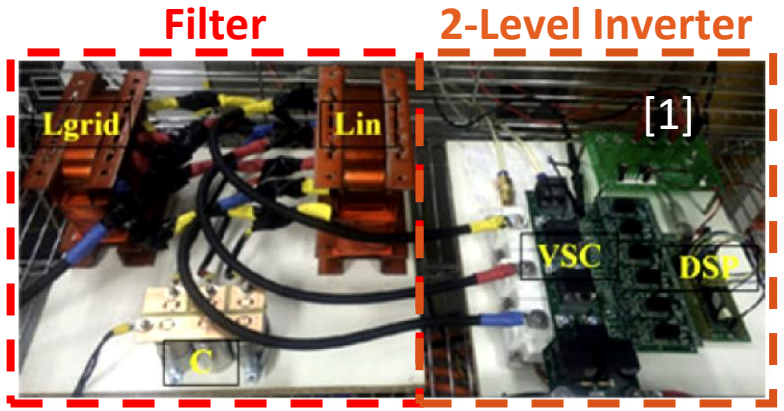
Course module on multilevel converters and electric vehicles in FA2019 power electronics class

Course module on multilevel converters and electric vehicles in SP2020 power systems class

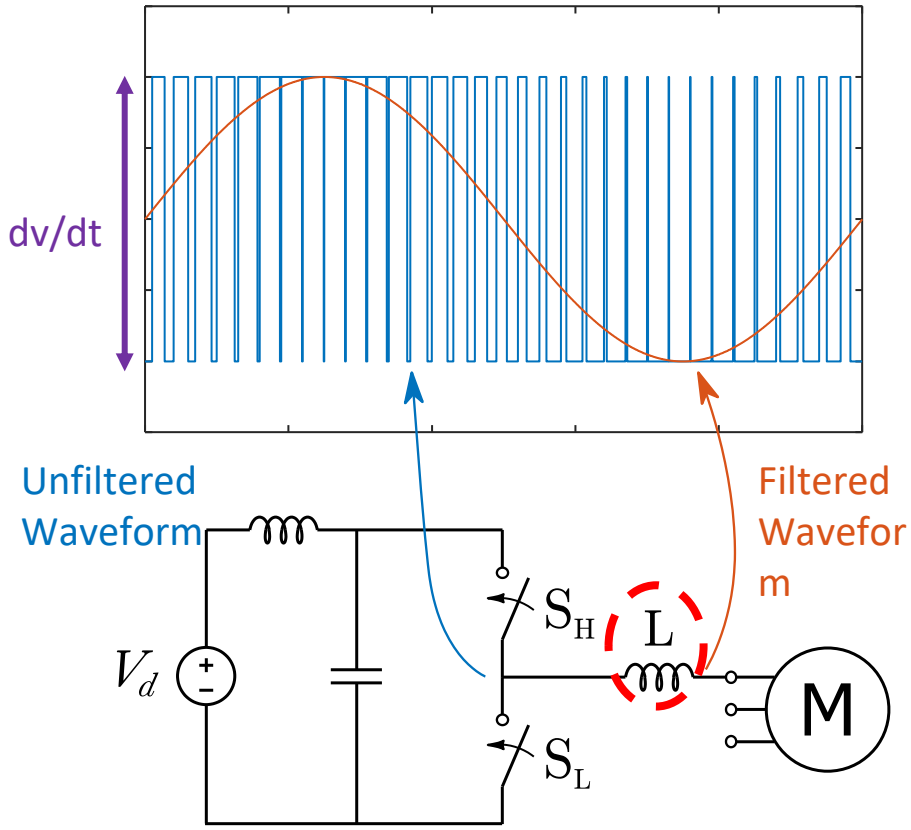
Back-Up Slides Next

Traditional Approach

- 2-level converters have been the standard approach
  - Requires large inductive filters (dv/dt limiter)
  - Increased motor losses due to harmonic
  - Large bus capacitance required



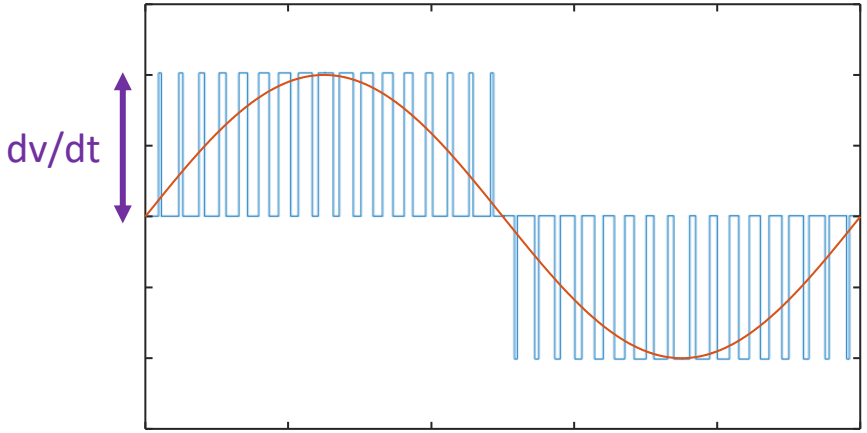
  - Custom power modules and gate drivers
  - Typically low redundancy [2]
  - Cooling can be challenging due to hot-spots

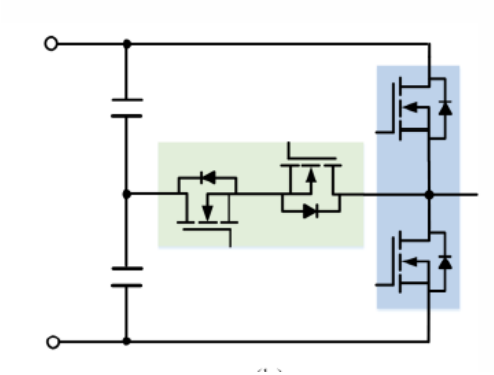


[1] Liu, et al., "LCL Filter Design of a 50-kW 60-kHz SiC Inverter with Size and Thermal Considerations for Aerospace Applications," IEEE TIE, 2017.
[2] E. Gurpinar, et al., "SiC MOSFET-Based Power Module Design and Analysis for EV Traction Systems," IEEE ECCE, 2018.

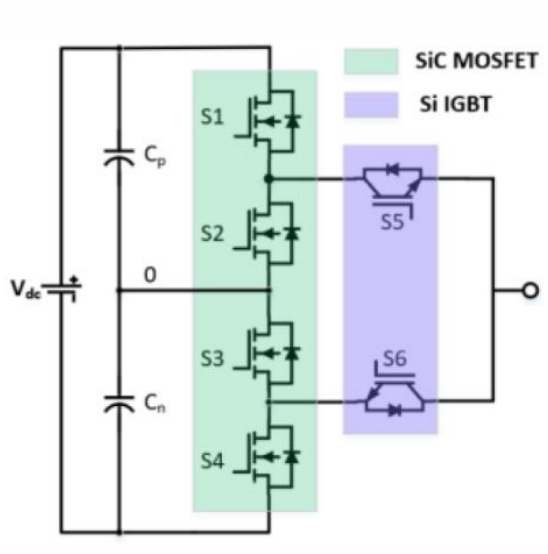
Traditional Approach

- 3-level neutral-point-clamp (NPC) topologies can reduce dv/dt
  - Similar design strategy as 2-level designs
  - Still require HV devices, high dv/dt





T-type NPC Phase Leg [4]



Active NPC Phase Leg [5]

– Both still require large volume/mass of filter magnetics at the output

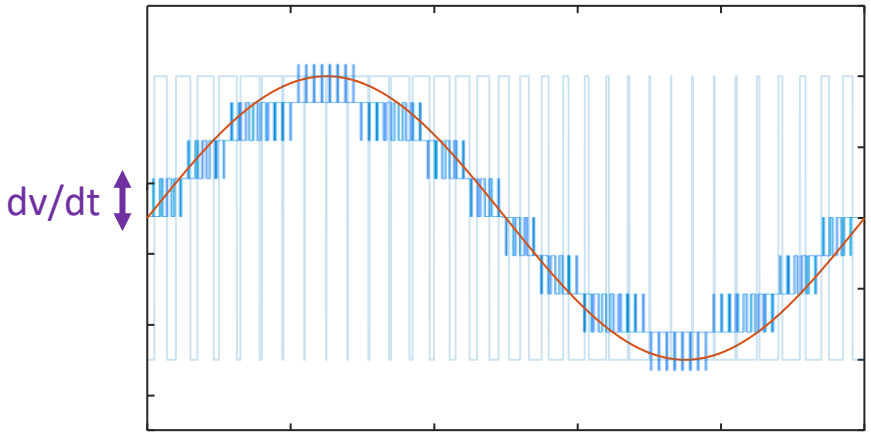
[3] Z. Wang, et. al, "Design and Validation of A 250 kW All Silicon Carbide High-Density Three-Level T-Type Inverter," IEEE JESTPE, 2019
[4] D. Pan, et al., "Control of MW-Scale High-Frequency "SiC+Si" Multilevel ANPC Inverter … for Aircraft … Applications," IEEE JESTPE, 2020

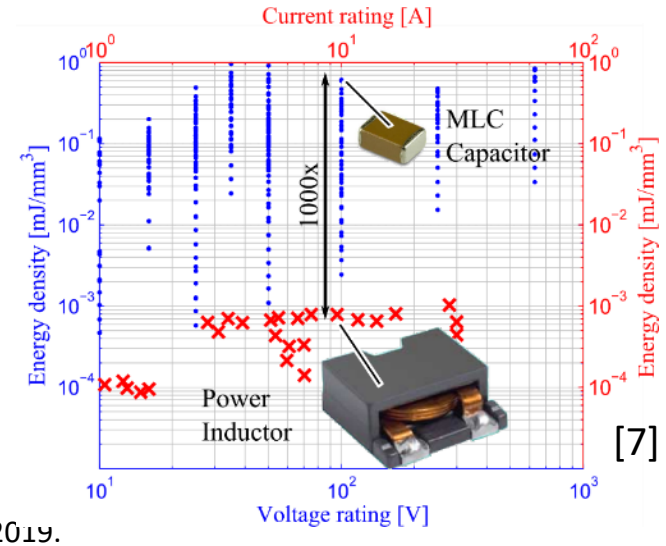
An Unconventional Approach

- Flying Capacitor Multilevel Converter
  - Low dv/dt with high level count
  - High effective switching frequency

Key Benefit [6]	2-Level	FCML
Switch Stress		
V_{sw} Ripple Amplitude		
V_{sw} Ripple Frequency		
Output Inductance		

- Allows the use of lower-cost, low-voltage WBG devices
- Energy dense capacitors process most of the converter energy





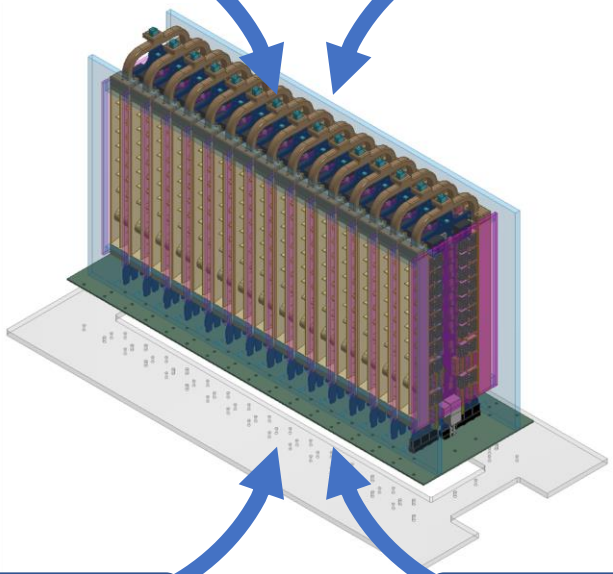
[7]

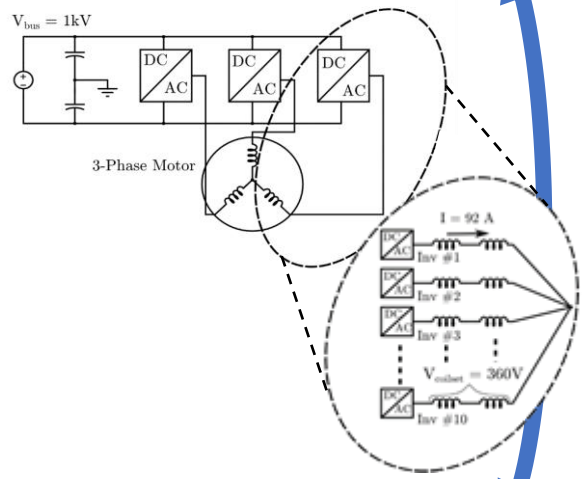
[5] C T. Meynard and H. Foch, "Multilevel conversion: high voltage choppers and voltage-source inverters," IEEE PESC, 1992.
[6] C. B. Barth, et. al, "Experimental Evaluation of Capacitors for Power Buffering in Single-Phase Power Converters," IEEE TPE, 2019.

Overall Approach

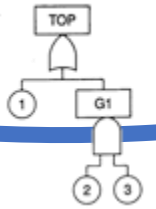
High-Performance Inverter Design and Modeling

Dynamics & Control of FCML Inverter Module





Reliability Assessment and FDI for FCML

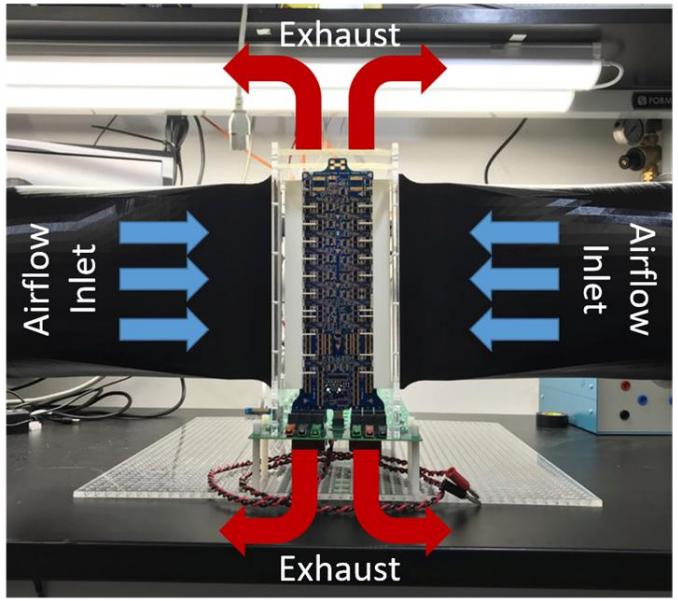


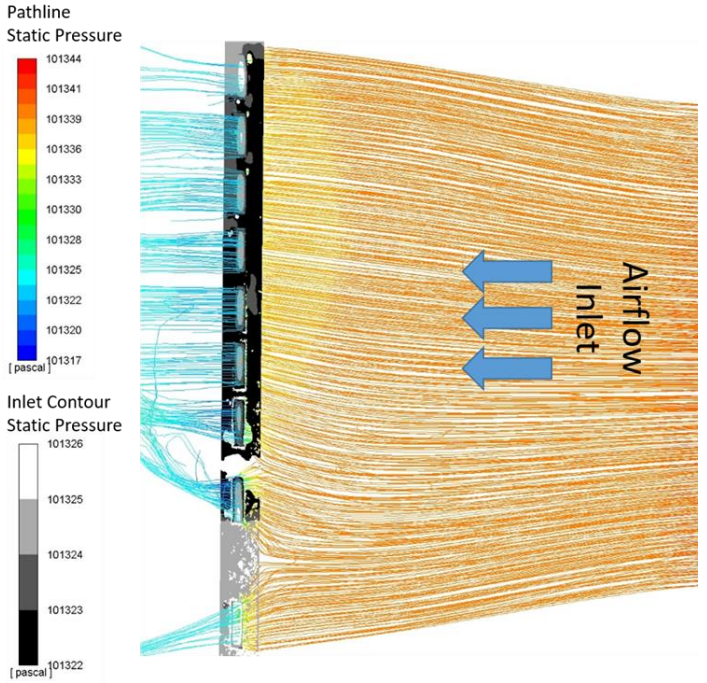
Scalability and Paralleling of Inverter Modules

Approach – Thermal Design

- Design of 3D-printed baffles and inlet ducts to guide flowing air
  - Ensures air is directed through heatsinks
- CFD simulation to ensure uniform pressure front at inlets of converter
  - Allows for optimization of inlet duct design

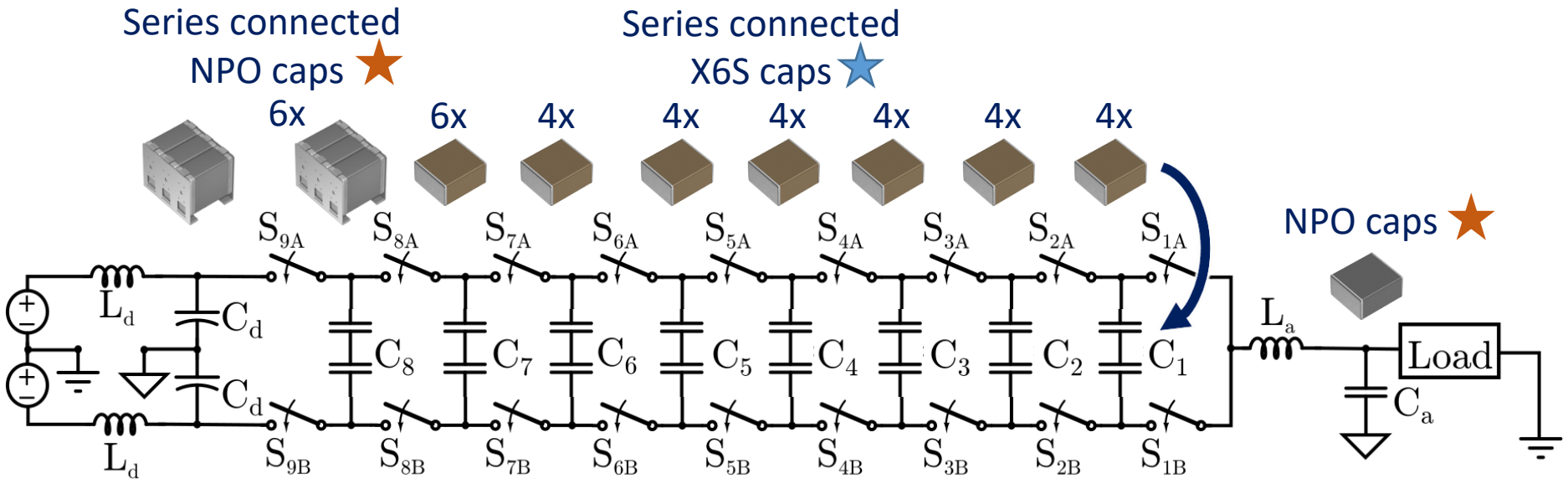
Current air-cooled test setup with inlet ducts directing air through baffles





CFD indicates negligible pressure or temperature difference across heat sinks

Capacitor Selection for 1kV Design



	DC Bus		C_8	C_7	C_6	C_5	C_4	C_3	C_2	C_1
Technology	Film	Series NPO 630V				Series X6S 450V				
Nominal DC Voltage [V]	1000	1000	889	778	667	556	444	333	222	111
Nominal Capacitance [µF]	56.4	2	1.1	6.6	4.4	4.4	4.4	4.4	4.4	4.4
Derated Capacitance [µF]	56.4	2	1.1	1.3	1.0	1.2	1.4	1.8	2.4	3.5

Loss Modeling Update

- Previously
  - Set output power
  - Generate current and voltage waveforms
  - Loop through time steps
  - Sum losses at steps along fundamental
- Current attempt
  - Set output impedance (real and imaginary)
  - Add losses at the switching frequency and harmonics for capacitor/inductor losses
  - Close loop on thermal
  - Close loop on output voltage drop due to loss